FAIRCHILD SEMICONDUCTOR®

March 2013

FSAM75SM60A
Motion SPM® 2 Series

Features

• UL Certified No. E209204

• 600 V-75 A 3-Phase IGBT Inverter Bridge Including Control ICs for Gate Driving and Protection

• Three Separate Negative DC-Link Terminals for Inverter Current Sensing Applications

• Single-Grounded Power Supply Thanks to Built-in HVIC

• Typical Switching Frequency of 5 kHz

• Built-in Thermistor for Temperature Monitoring

• Inverter Power Rating of 0.8 kW / 100~253 VAC

• Isolation Rating of 2500 Vrms/min.

• Very Low Leakage Current by Using Ceramic Substrate

• Adjustable Current Protection Level by Changing The Value of Series Resistor Connected to The Emitters of Sense-IGBT

• RoHS compliant Applications

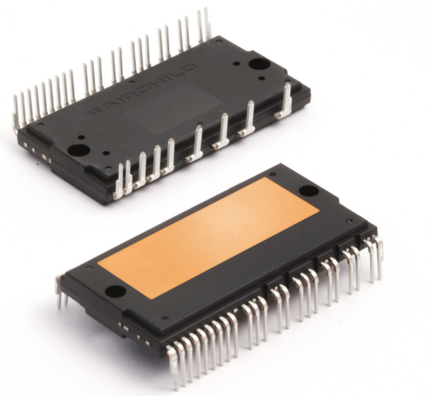
• Motion Control - Home Appliance/Industrial MotorFeatures

General Description

FSAM75SM60A is a Motion SPM 2 series That Fairchild Has Developed to Provide a Very Compact and Low Cost, Yet High Performance Inverter Solution for AC Motor Drives in Low-Power Applications Such as Air Conditioners. It Combines Optimized Circuit Protections and Drive Matched to Low-Loss IGBTs. Effective Over-Current Protection is Realized Through Advanced Current Sensing IGBTs. The System Reliability is Further Enhanced by The Built-in Thermistor and Integrated Under-voltage Lock-out Protection. In Addition The Incorporated HVIC Facilitates The Use of Single-Supply Voltage Without Any Negative Bias. Inverter Leg Current Sensing Can Be Implemented Because of Three Separate Nagative DC Terminals.

Resource

• AN-9043 : Motion SPM® 2 Series User's Guide



Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Packing Type	Quantity
FSAM75SM60A	FSAM75SM60A	S32DA-032	-	RAIL	8

Integrated Power Functions

- 600V-75A IGBT inverter for three-phase DC/AC power conversion (Please refer to Fig. 3)

Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting
  Control circuit under-voltage (UV) protection
  Note) Available bootstrap circuit example is given in Figs. 13 and 14.
- For inverter low-side IGBTs: Gate drive circuit, Short circuit protection (SC)
  Control supply circuit under-voltage (UV) protection
- Temperature Monitoring: System over-temperature monitoring using built-in thermistor
  Note) Available temperature monitoring circuit is given in Fig. 14.
- Fault signaling: Corresponding to a SC fault (Low-side IGBTs) or a UV fault (Low-side control supply circuit)
- Input interface: Active - Low Interface, Can Work with 3.3/5 V Logic

Pin Configuration

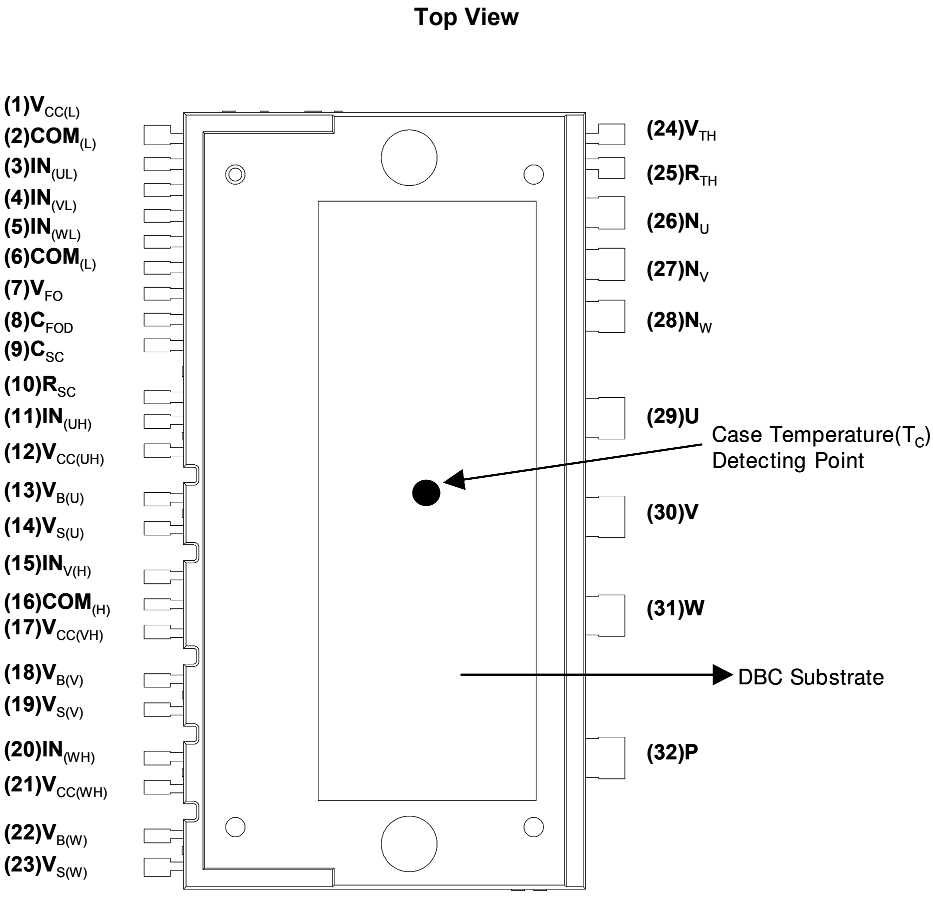
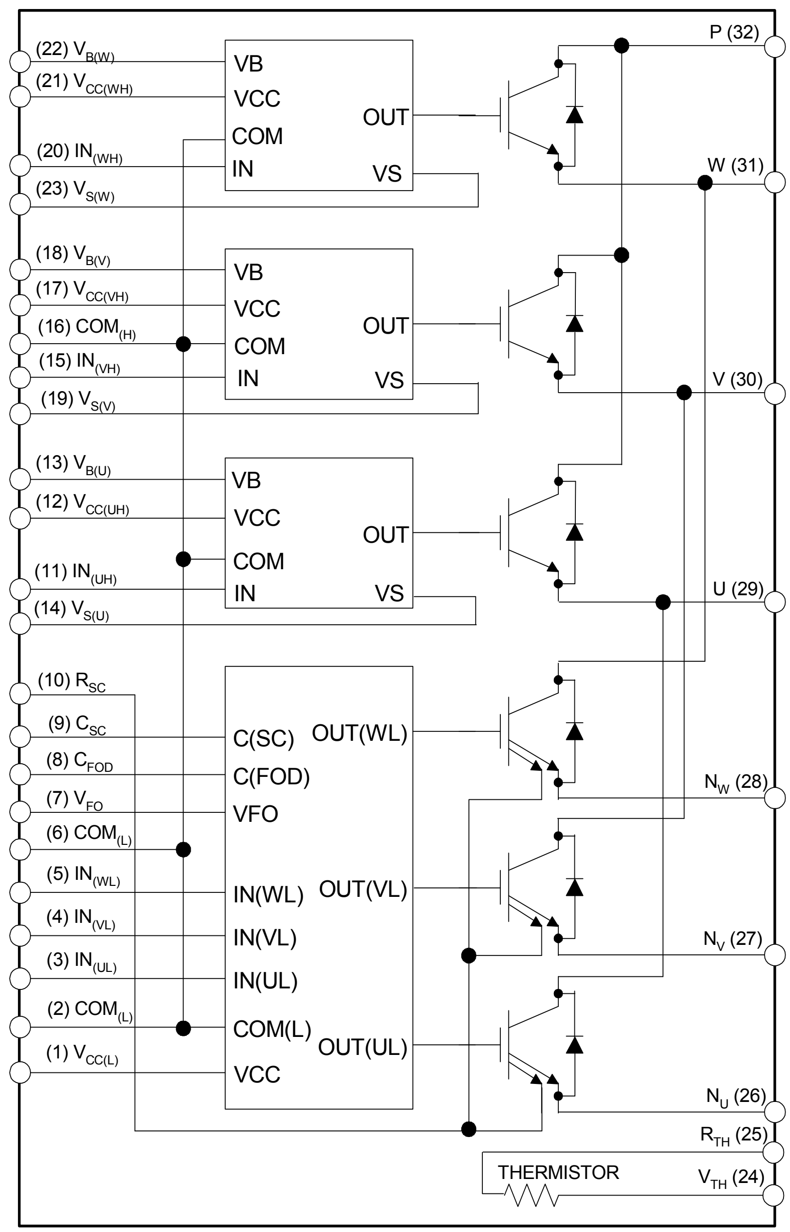


Fig. 2.

Pin Descriptions

Pin Number	Pin Name	Pin Description
1	$V_{CC(L)}$	Low-side Common Bias Voltage for IC and IGBTs Driving
2	$COM_{(L)}$	Low-side Common Supply Ground
3	$IN_{(UL)}$	Signal Input Terminal for Low-side U Phase
4	$IN_{(VL)}$	Signal Input Terminal for Low-side V Phase
5	$IN_{(WL)}$	Signal Input Terminal for Low-side W Phase
6	$COM_{(L)}$	Low-side Common Supply Ground
7	V_{FO}	Fault Output
8	C_{FOD}	Capacitor for Fault Output Duration Time Selection
9	C_{SC}	Capacitor (Low-pass Filter) for Short-Circuit Current Detection Input
10	R_{SC}	Resistor for Short-circuit Current Detection
11	$IN_{(UH)}$	Signal Input for High-side U Phase
12	$V_{CC(UH)}$	High-side Bias Voltage for U Phase IC
13	$V_{B(U)}$	High-side Bias Voltage for U Phase IGBT Driving
14	$V_{S(U)}$	High-side Bias Voltage Ground for U Phase IGBT Driving
15	$IN_{(VH)}$	Signal Input for High-side V Phase
16	$COM_{(H)}$	High-side Common Supply Ground
17	$V_{CC(VH)}$	High-side Bias Voltage for V Phase IC
18	$V_{B(V)}$	High-side Bias Voltage for V Phase IGBT Driving
19	$V_{S(V)}$	High-side Bias Voltage Ground for V Phase IGBT Driving
20	$IN_{(WH)}$	Signal Input for High-side W Phase
21	$V_{CC(WH)}$	High-side Bias Voltage for W Phase IC
22	$V_{B(W)}$	High-side Bias Voltage for W Phase IGBT Driving
23	$V_{S(W)}$	High-side Bias Voltage Ground for W Phase IGBT Driving
24	V_{TH}	Thermistor Bias Voltage
25	R_{TH}	Series Resistor for the Use of Thermistor (Temperature Detection)
26	N_U	Negative DC–Link Input Terminal for U Phase
27	N_V	Negative DC–Link Input Terminal for V Phase
28	N_W	Negative DC–Link Input Terminal for W Phase
29	U	Output for U Phase
30	V	Output for V Phase
31	W	Output for W Phase
32	P	Positive DC–Link Input

Internal Equivalent Circuit and Input/Output Pins



Note

1. Inverter low-side is composed of three sense-IGBTs including freewheeling diodes for each IGBT and one control IC which has gate driving, current sensing and protection functions.
2. Inverter power side is composed of four inverter dc-link input pins and three inverter output pins.
3. Inverter high-side is composed of three normal-IGBTs including freewheeling diodes and three drive ICs for each IGBT.

Fig. 3.

Absolute Maximum Ratings (T_J = 25°C, Unless Otherwise Specified)

Inverter Part

Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DC}	Applied to DC - Link	450	V
Supply Voltage (Surge)	$V_{PN(Surge)}$	Applied between P- N	500	V
Collector-emitter Voltage	V_{CES}		600	V
Each IGBT Collector Current	$\pm I_C$	T_C = 25°C	75	A
Each IGBT Collector Current	$\pm I_C$	T_C = 100°C	37	A
Each IGBT Collector Current (Peak)	$\pm I_{CP}$	T_C = 25°C , Under 1ms pulse width	110	A
Collector Dissipation	P_C	T_C = 25°C per One Chip	189	W
Operating Junction Temperature	T_J	(Note 1)	-20 ~ 125	°C

Note
1. It would be recommended that the average junction temperature should be limited to $T_J \leq$ 125°C (@$T_C \leq$ 100°C) in order to guarantee safe operation.

Control Part

Item	Symbol	Condition	Rating	Unit
Control Supply Voltage	V_{CC}	Applied between $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$ - $COM_{(H)}$, $V_{CC(L)}$ - $COM_{(L)}$	20	V
High-side Control Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	20	V
Input Signal Voltage	V_{IN}	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$ $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$	-0.3 ~ V_{CC}+0.3	V
Fault Output Supply Voltage	V_{FO}	Applied between V_{FO} - $COM_{(L)}$	-0.3 ~ V_{CC}+0.3	V
Fault Output Current	I_{FO}	Sink Current at V_{FO} Pin	5	mA
Current Sensing Input Voltage	V_{SC}	Applied between C_{SC} - $COM_{(L)}$	-0.3 ~ V_{CC}+0.3	V

Total System

Item	Symbol	Condition	Rating	Unit
Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{PN(PROT)}$	Applied to DC - Link, V_{CC} = V_{BS} = 13.5 ~ 16.5 V T_J = 125°C, Non-repetitive, less than 5μs	400	V
Module Case Operation Temperature	T_C	Note Fig. 2	-20 ~ 100	°C
Storage Temperature	T_{STG}		-20 ~ 125	°C
Isolation Voltage	V_{ISO}	60Hz, Sinusoidal, AC 1 minute, Connection Pins to Heat-sink Plate	2500	V_{rms}

Absolute Maximum Ratings

Thermal Resistance

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6 module)	-	-	0.56	°C/W
	$R_{th(j-c)F}$	Inverter FWDi part (per 1/6 module)	-	-	0.98	°C/W
Contact Thermal Resistance	$R_{th(c-f)}$	Ceramic Substrate (per 1 Module) Thermal Grease Applied (Note 3)	-	-	0.06	°C/W

Note

2. For the measurement point of case temperature(T_C), please refer to Fig. 2.
3. The thickness of thermal grease should not be more than 100um.

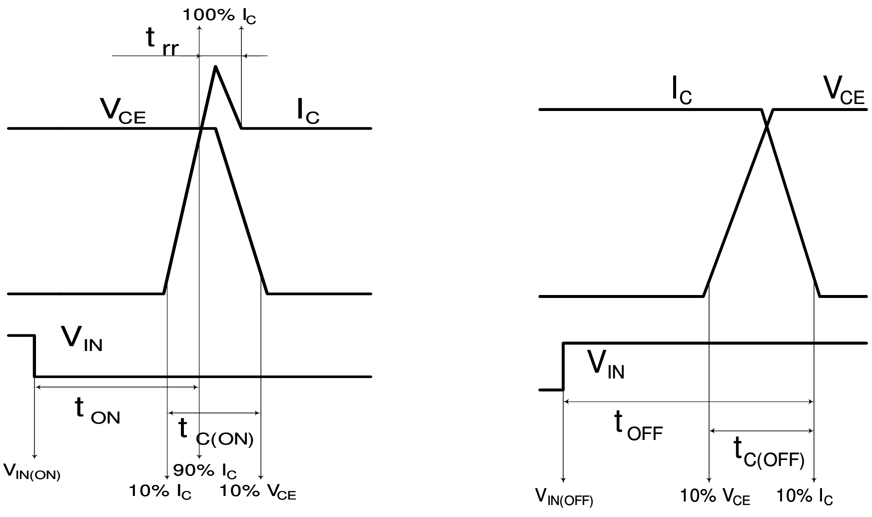
Electrical Characteristics

Inverter Part (T_J = 25°C, Unless Otherwise Specified)

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector - emitter Saturation Voltage	$V_{CE(SAT)}$	$V_{CC} = V_{BS}$ = 15 V V_{IN} = 0 V	I_C = 50 A, T_J = 25°C	-	-	2.4	V
FWDi Forward Voltage	V_{FM}	V_{IN} = 5 V	I_C = 50 A, T_J = 25°C	-	-	2.1	V
Switching Times	t_{ON}	V_{PN} = 300 V, $V_{CC} = V_{BS}$ = 15 V I_C = 75 A, T_J = 25°C V_{IN} = 5 V ↔ 0 V, Inductive Load (High-Low Side) (Note 4)		-	0.76	-	µs
	$t_{C(ON)}$			-	0.44	-	µs
	t_{OFF}			-	1.42	-	µs
	$t_{C(OFF)}$			-	0.46	-	µs
	t_{rr}			-	0.10	-	µs
Collector - emitter Leakage Current	I_{CES}	$V_{CE} = V_{CES}$, T_J = 25°C		-	-	250	µA

Note

4. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Fig. 4.



(a) Turn-on

(b) Turn-off

Fig. 4. Switching Time Definition

Electrical Characteristics (T_J = 25°C, Unless Otherwise Specified)

Control Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Quiescent V_{CC} Supply Current	I_{QCCL}	V_{CC} = 15 V $IN_{(UL, VL, WL)}$ = 5V	$V_{CC(L)}$ - $COM_{(L)}$	-	-	26	mA
	I_{QCCH}	V_{CC} = 15 V $IN_{(UH, VH, WH)}$ = 5V	$V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$ - $COM_{(H)}$	-	-	130	uA
Quiescent V_{BS} Supply Current	I_{QBS}	V_{BS} = 15 V $IN_{(UH, VH, WH)}$ = 5V	$V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ -$V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	-	-	420	uA
Fault Output Voltage	V_{FOH}	V_{SC} = 0 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		4.5	-	-	V
	V_{FOL}	V_{SC} = 1 V, V_{FO} Circuit: 4.7 kΩ to 5 V Pull-up		-	-	1.1	V
Short-Circuit Trip Level	$V_{SC(ref)}$	V_{CC} = 15 V (Note 5)		0.45	0.51	0.56	V
Sensing Voltage of IGBT Current	V_{SEN}	R_{SC} = 26 Ω, R_{SU} = R_{SV} = R_{SW} = 0 Ω and I_C = 100A (Fig. 6)		0.45	0.51	0.56	V
Supply Circuit Under-Voltage Protection	UV_{CCD}	Detection Level		11.5	12	12.5	V
	UV_{CCR}	Reset Level		12	12.5	13	V
	UV_{BSD}	Detection Level		7.3	9.0	10.8	V
	UV_{BSR}	Reset Level		8.6	10.3	12	V
Fault Output Pulse Width	t_{FOD}	C_{FOD} = 33 nF (Note 6)		1.4	1.8	2.0	ms
ON Threshold Voltage	$V_{IN(ON)}$	High-Side	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$	-	-	0.8	V
OFF Threshold Voltage	$V_{IN(OFF)}$			3.0	-	-	V
ON Threshold Voltage	$V_{IN(ON)}$	Low-Side	Applied between $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$	-	-	0.8	V
OFF Threshold Voltage	$V_{IN(OFF)}$			3.0	-	-	V
Resistance of Thermistor	R_{TH}	@ T_{TH} = 25°C (Note Fig. 5) (Note 7)		-	50	-	kΩ
		@ T_{TH} = 100°C (Note Fig. 5) (Note 7)		-	3.0	-	kΩ

Note:
5. Short-circuit current protection is functioning only at the low-sides. It would be recommended that the value of the external sensing resistor (R_{SC}) should be selected around 26 Ω in order to make the SC trip-level of about 100A at the shunt resistors (R_{SU},R_{SV},R_{SW}) of 0Ω . For the detailed information about the relationship between the external sensing resistor (R_{SC}) and the shunt resistors (R_{SU},R_{SV},R_{SW}), please see Fig. 6.
6. The fault-out pulse width t_{FOD} depends on the capacitance value of C_{FOD} according to the following approximate equation : $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}$[F]
7. T_{TH} is the temperature of thermistor itself. To know case temperature (T_C), please make the experiment considering your application.

Recommended Operating Conditions

Item	Symbol	Condition	Values			Unit
			Min.	Typ.	Max.	
Supply Voltage	V_{PN}	Applied between P - N_U, N_V, N_W	-	300	400	V
Control Supply Voltage	V_{CC}	Applied between $V_{CC(UH)}$, $V_{CC(VH)}$, $V_{CC(WH)}$ - $COM_{(H)}$, $V_{CC(L)}$ - $COM_{(L)}$	13.5	15	16.5	V
High-side Bias Voltage	V_{BS}	Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$	13.0	15	18.5	V
Blanking Time for Preventing Arm-short	t_{dead}	For Each Input Signal	3.5	-	-	us
PWM Input Signal	f_{PWM}	$T_C \le 100°C$, $T_J \le 125°C$	-	5	-	kHz
Minimum Input Pulse Width	$PW_{IN(OFF)}$	$200 \le V_{PN} \le 400$ V, $13.5 \le V_{CC} \le 16.5$ V, $13.0 \le V_{BS} \le 18.5$ V, $0 \le I_C \le 110$ A, $-20 \le T_J \le 125°C$ V_{IN} = 5 V ↔ 0 V, Inductive Load (Note 8)	3	-	-	us
Input ON Threshold Voltage	$V_{IN(ON)}$	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$	0 ~ 0.65			V
Input OFF Threshold Voltage	$V_{IN(OFF)}$	Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$ - $COM_{(H)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - $COM_{(L)}$	4 ~ 5.5			V

Note:
8. SPM might not make response if the $PW_{IN(OFF)}$ is less than the recommended minimum value.

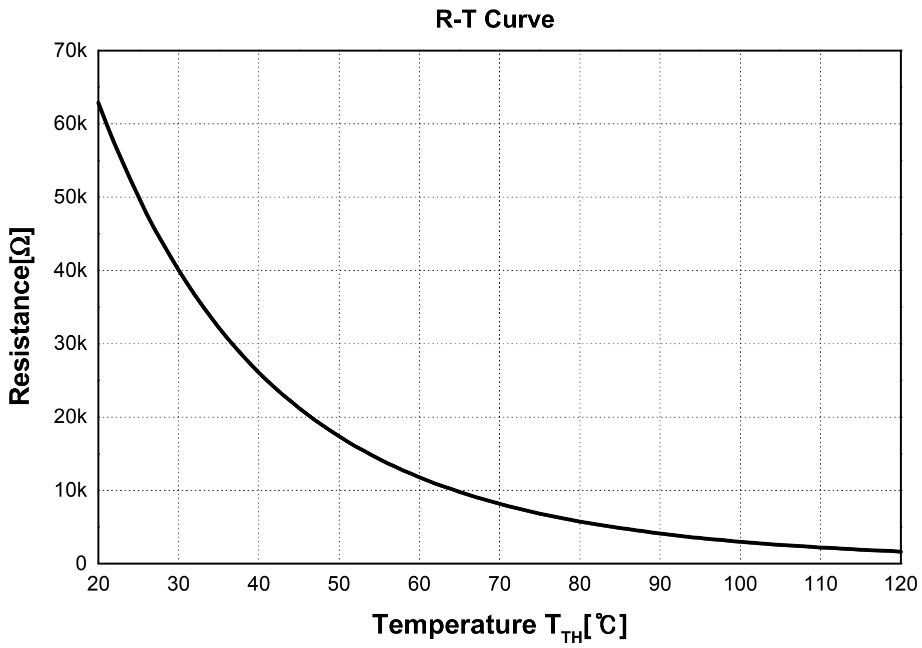


Fig. 5. R-T Curve of The Built-in Thermistor

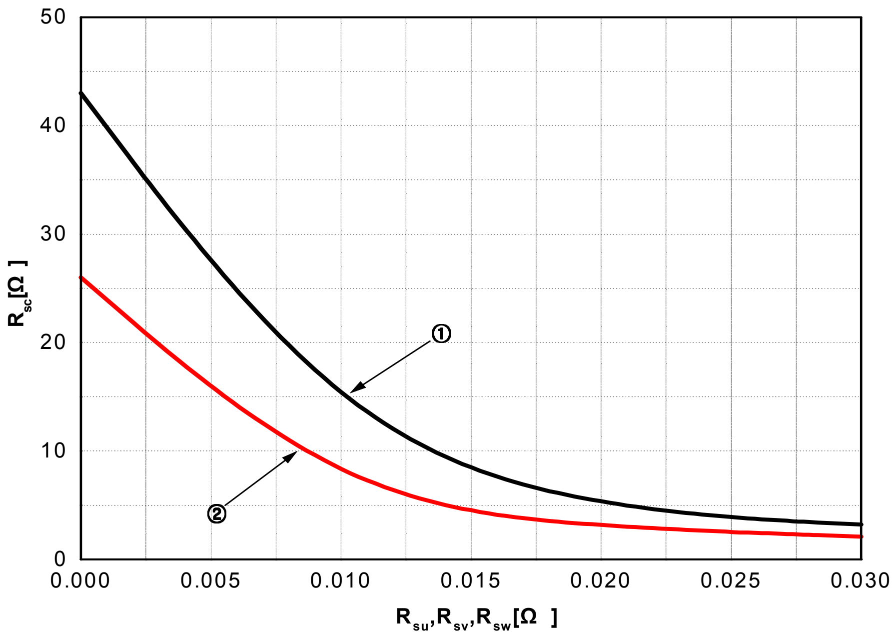


Fig. 6. R_{SC} Variation by change of Shunt Resistors (R_{SU}, R_{SV}, R_{SW}) for Short-Circuit Protection
① @ Current Trip Level ≒ 75 A,
② @ Current Trip Level ≒ 100 A

Mechanical Characteristics and Ratings

Item	Condition		Limits Min.	Limits Typ.	Limits Max.	Units
Mounting Torque	Mounting Screw: M4 (Note 9 and 10)	Recommended 10 Kg•cm	8	10	12	Kg•cm
		Recommended 0.98 N•m	0.78	0.98	1.17	N•m
DBC Flatness		Note Fig.7	0	-	+120	µm
Weight			-	32	-	g

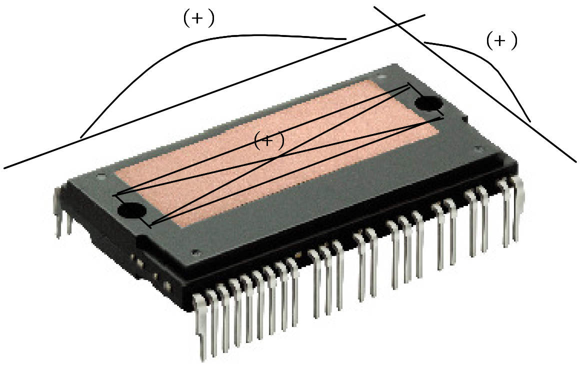


Fig. 7. Flatness Measurement Position of The DBC Substrate

Note:
9. Do not make over torque or mounting screws. Much mounting torque may cause ceramic cracks and bolts and Al heat-fin destruction.
10. Avoid one side tightening stress. Fig.8 shows the recommended torque order for mounting screws. Uneven mounting can cause the SPM ceramic substrate to be damaged.

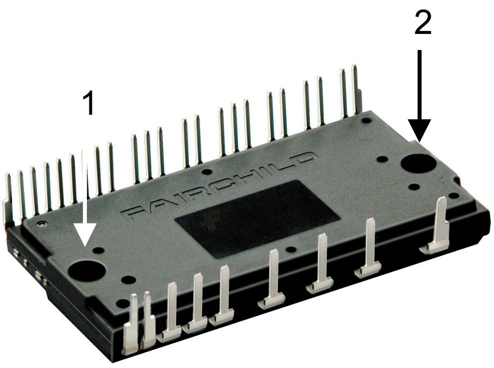
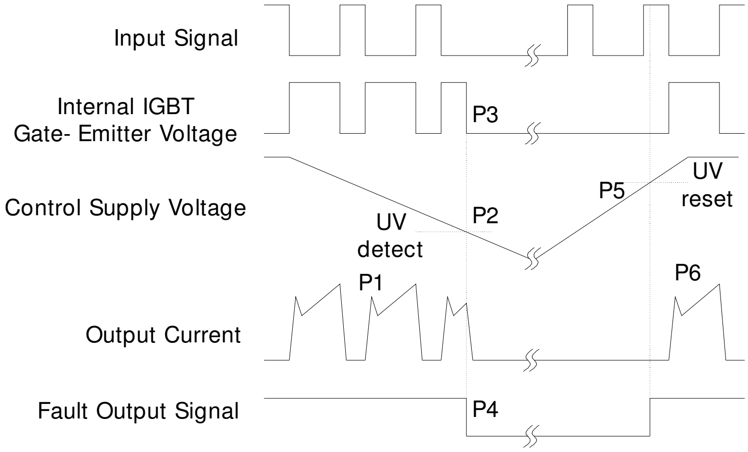


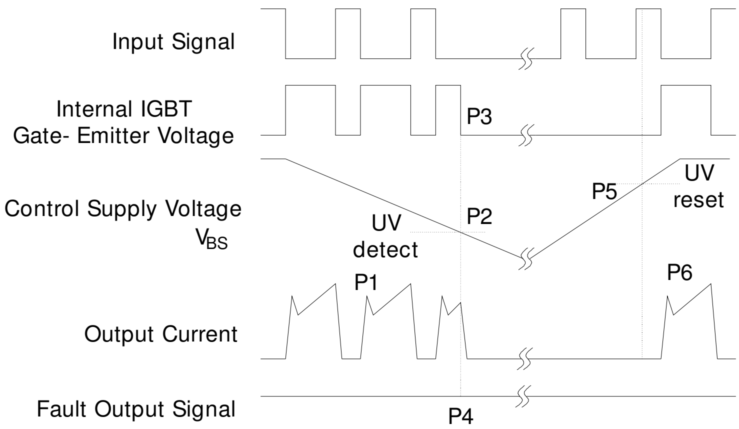
Fig. 8. Mounting Screws Torque Order (1 → 2)

Time Charts of SPM® Protective Function



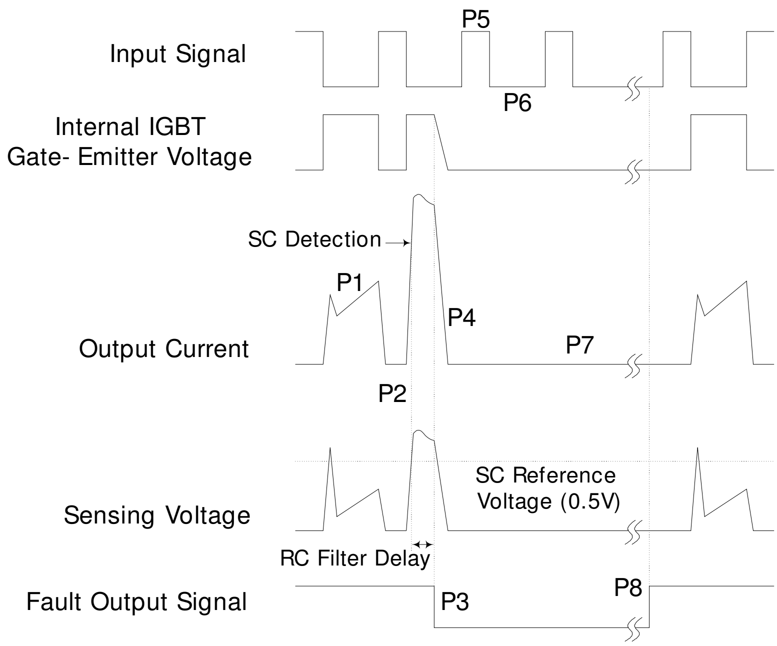
P1 : Normal operation - IGBT ON and conducting current
P2 : Under voltage detection
P3 : IGBT gate interrupt
P4 : Fault signal generation
P5 : Under voltage reset
P6 : Normal operation - IGBT ON and conducting current

Fig. 9. Under-Voltage Protection (Low-side)



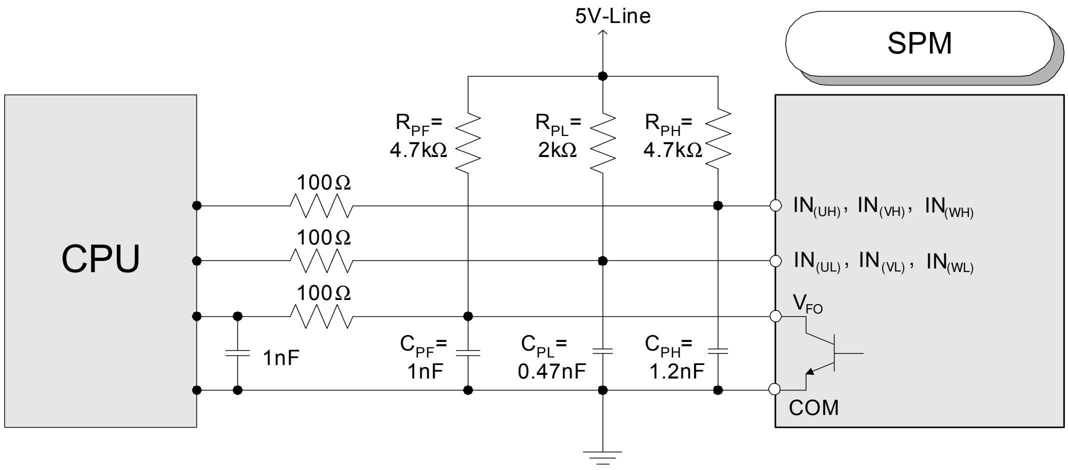
P1 : Normal operation - IGBT ON and conducting current
P2 : Under voltage detection
P3 : IGBT gate interrupt
P4 : No fault signal
P5 : Under voltage reset
P6 : Normal operation - IGBT ON and conducting current

Fig. 10. Under-Voltage Protection (High-side)



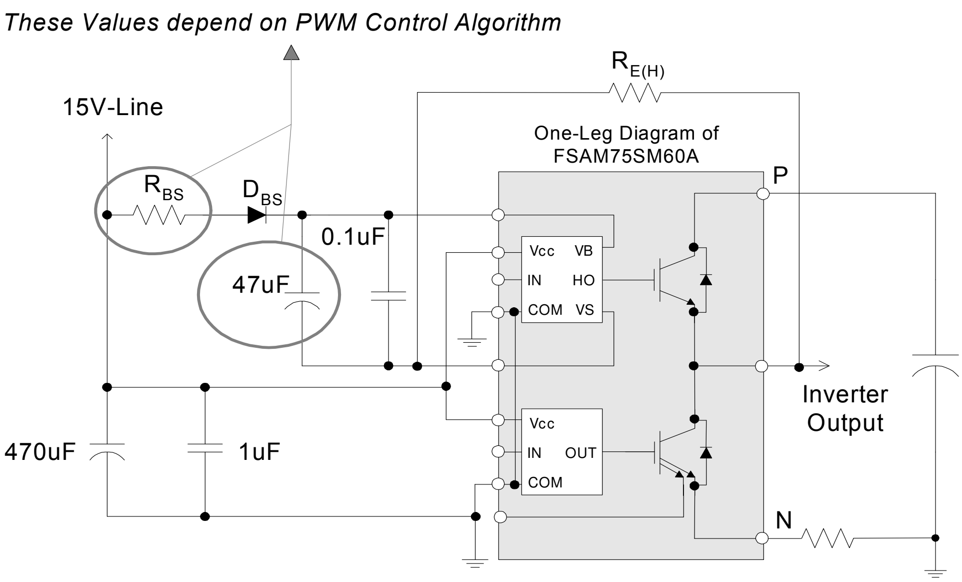
P1 : Normal operation - IGBT ON and conducting currents
P2 : Short-circuit current detection
P3 : IGBT gate interrupt / Fault signal generation
P4 : IGBT is slowly turned off
P5 : IGBT OFF signal
P6 : IGBT ON signal - but IGBT cannot be turned on during the fault-output activation
P7 : IGBT OFF state
P8 : Fault-output reset and normal operation start

Fig. 11. Short-circuit Current Protection (Low-side Operation only)



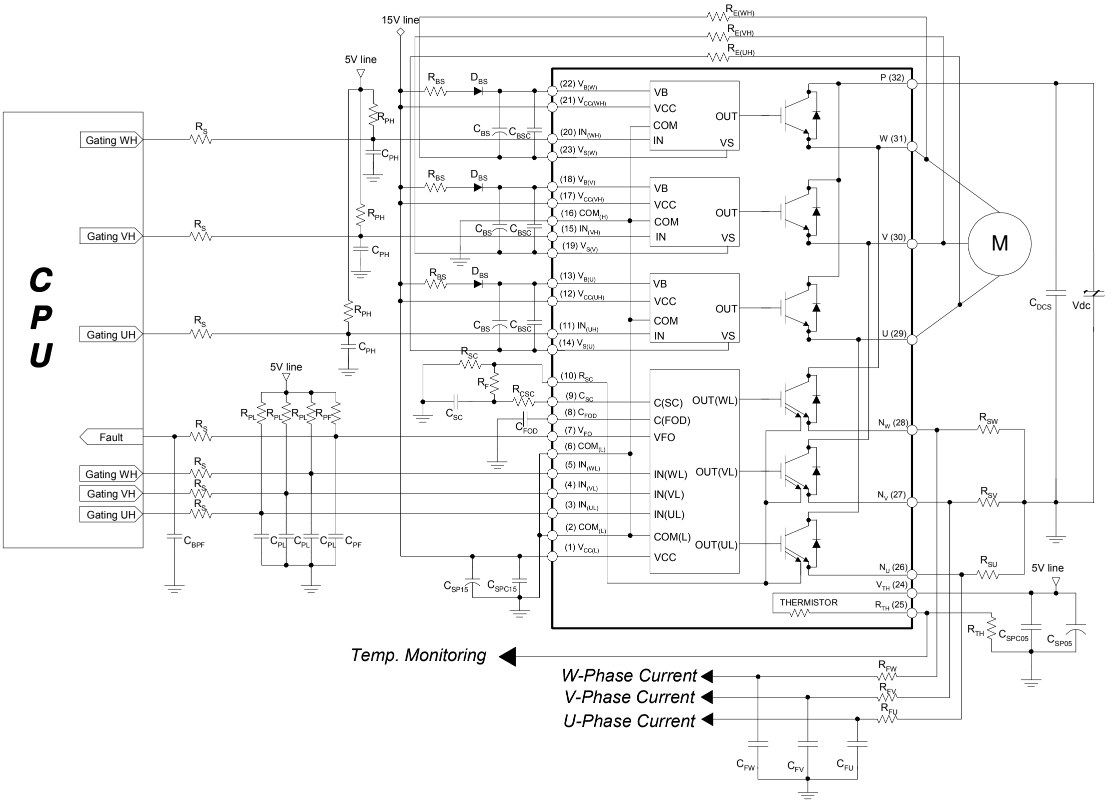
Note:
1) It would be recommended that by-pass capacitors for the gating input signals, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$, $IN_{(UH)}$, $IN_{(VH)}$ and $IN_{(WH)}$ should be placed on the SPM pins and on the both sides of CPU and SPM for the fault output signal, V_{FO}, as close as possible.
2) The logic input is compatible with standard CMOS or LSTTL outputs.
3) $R_{PL}C_{PL}/R_{PH}C_{PH}/R_{PF}C_{PF}$ coupling at each SPM input is recommended in order to prevent input/output signals' oscillation and it should be as close as possible to each of SPM pins.

Fig. 12. Recommended CPU I/O Interface Circuit



Note:
1) It would be recommended that the bootstrap diode, D_{BS}, has soft and fast recovery characteristics.
2) The bootstrap resistor (R_{BS}) should be 3 times greater than $R_{E(H)}$. The recommended value of $R_{E(H)}$ is 5.6Ω, but it can be increased up to 20Ω for a slower dv/dt of high-side.
3) The ceramic capacitor placed between V_{CC}-COM should be over 1μF and mounted as close to the pins of the SPM as possible.

Fig. 13. Recommended Bootstrap Operation Circuit and Parameters



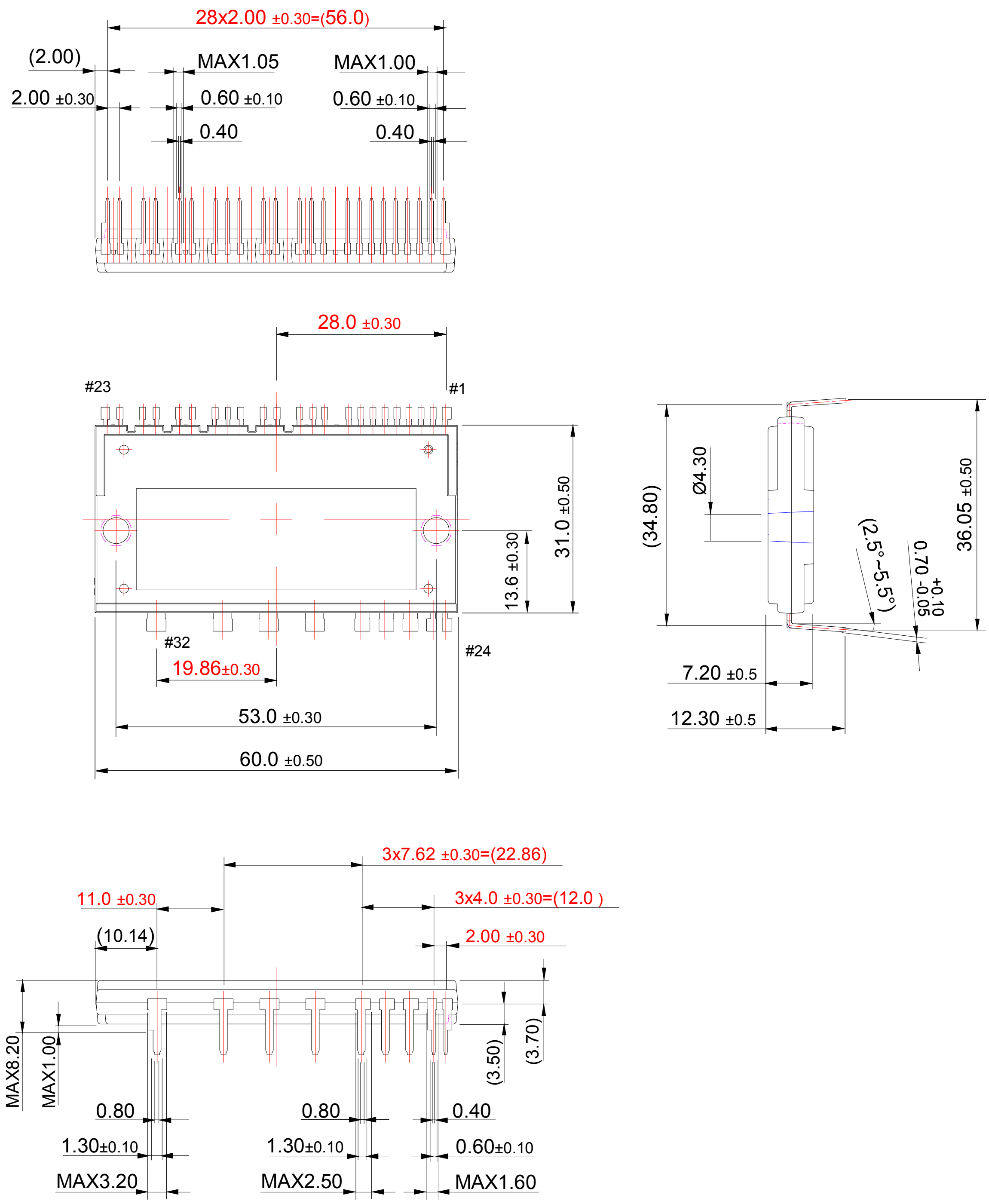
Note:

1) $R_{PL}C_{PL}/R_{PH}C_{PH}$ /$R_{PF}C_{PF}$ coupling at each SPM input is recommended in order to prevent input signals' oscillation and it should be as close as possible to each SPM input pin.
2) By virtue of integrating an application specific type HVIC inside the SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.
3) V_{FO} output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7kΩ resistance. Please refer to Fig. 12.
4) C_{SP15} of around 7 times larger than bootstrap capacitor C_{BS} is recommended.
5) V_{FO} output pulse width should be determined by connecting an external capacitor(C_{FOD}) between C_{FOD}(pin8) and $COM_{(L)}$(pin2). (Example : if C_{FOD} = 33 nF, then t_{FO} = 1.8 ms (typ.)) Please refer to the note 6 for calculation method.
6) Each input signal line should be pulled up to the 5V power supply with approximately 4.7kΩ (at high side input) or 2kΩ (at low side input) resistance (other RC coupling circuits at each input may be needed depending on the PWM control scheme used and on the wiring impedance of the system's printed circuit board). Approximately a 0.22~2nF by-pass capacitor should be used across each power supply connection terminals.
7) To prevent errors of the protection function, the wiring around R_{SC}, R_F and C_{SC} should be as short as possible.
8) In the short-circuit protection circuit, please select the R_FC_{SC} time constant in the range 3~4 μs.
9) Each capacitor should be mounted as close to the pins of the SPM as possible.
10) To prevent surge destruction, the wiring between the smoothing capacitor and the P&N pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22 μF between the P&N pins is recommended.
11) Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays. It is recommended that the distance be 5cm at least.

Fig. 14. Application Circuit

Detailed Package Outline Drawings

SPM32-DA



Dimmensions in Millimeters

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CROSSVOLT™
CTL™
Current Transfer Logic™
DEUXPEED®
Dual Cool™
EcoSPARK®
EfficientMax™
ESBC™
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Fairchild®
Fairchild Semiconductor®
FACT Quiet Series™
FACT®
FAST®
FastvCore™
FETBench™
FPS™
F-PFS™
FRFET®
Global Power Resource℠
GreenBridge™
Green FPS™
Green FPS™ e-Series™
Gmax™
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IntelliMAX™
ISOPLANAR™
Making Small Speakers Sound Louder and Better™
MegaBuck™
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MicroFET™
MicroPak™
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TinyBoost™
TinyBuck™
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Definition of Terms

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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
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