

# FQL40N50F

## 500V N-Channel MOSFET

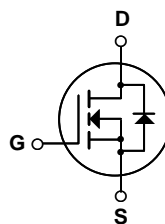
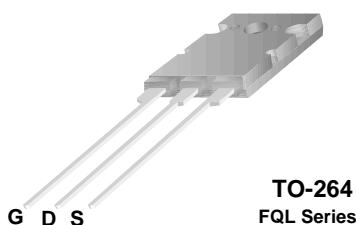
### General Description

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies, where the body diode is used such as phase-shift ZVS, basic full-bridge topology.

### Features

- 40A, 500V,  $R_{DS(on)} = 0.11\Omega @ V_{GS} = 10V$
- Low gate charge ( typical 155 nC)
- Low Crss ( typical 95 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability
- Fast recovery body diode ( max, 250ns )



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	FQL40N50F	Units
V <sub>DSS</sub>	Drain-Source Voltage	500	V
I <sub>D</sub>	Drain Current - Continuous (T <sub>C</sub> = 25°C) - Continuous (T <sub>C</sub> = 100°C)	40	A
		25	A
I <sub>DM</sub>	Drain Current - Pulsed (Note 1)	160	A
V <sub>GSS</sub>	Gate-Source Voltage	± 30	V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	1800	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	40	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	46	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns
P <sub>D</sub>	Power Dissipation (T <sub>C</sub> = 25°C) - Derate above 25°C	460	W
		3.7	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
R <sub>θJC</sub>	Thermal Resistance, Junction-to-Case	--	0.27	°C/W
R <sub>θCS</sub>	Thermal Resistance, Case-to-Sink	0.1	--	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction-to-Ambient	--	30	°C/W

**Electrical Characteristics** $T_C = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	500	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.48	--	$\text{V}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	--	--	50	$\mu\text{A}$
		$V_{DS} = 400\text{ V}, T_C = 125^\circ\text{C}$	--	--	500	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA

**On Characteristics**

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 20\text{ A}$	--	0.085	0.11	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 50\text{ V}, I_D = 20\text{ A}$ (Note 4)	--	29	--	S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	5800	7500	pF
$C_{oss}$	Output Capacitance		--	880	1150	pF
$C_{riss}$	Reverse Transfer Capacitance		--	95	120	pF

**Switching Characteristics**

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{ V}, I_D = 40\text{ A},$ $R_G = 25\ \Omega$	--	140	290	ns
$t_r$	Turn-On Rise Time		--	440	890	ns
$t_{d(off)}$	Turn-Off Delay Time		--	350	700	ns
$t_f$	Turn-Off Fall Time		(Note 4, 5)	--	250	500
$Q_g$	Total Gate Charge	$V_{DS} = 400\text{ V}, I_D = 40\text{ A},$ $V_{GS} = 10\text{ V}$	--	155	200	nC
$Q_{gs}$	Gate-Source Charge		--	37	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4, 5)	--	78	--

**Drain-Source Diode Characteristics and Maximum Ratings**

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	40	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	160	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 40\text{ A}$	--	--	1.4	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 40\text{ A},$	--	--	250	ns
$Q_{rr}$	Reverse Recovery Charge	$di_F / dt = 100\text{ A}/\mu\text{s}$ (Note 4)	--	1.3	--	$\mu\text{C}$

**Notes:**

1. Repetitive Rating : Pulse width limited by maximum junction temperature
2.  $L = 2.0\text{mH}, I_{AS} = 40\text{A}, V_{DD} = 50\text{V}, R_G = 25\ \Omega$ , Starting  $T_J = 25^\circ\text{C}$
3.  $I_{SD} \leq 40\text{A}, di/dt \leq 450\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse Test : Pulse width  $\leq 300\ \mu\text{s}$ , Duty cycle  $\leq 2\%$
5. Essentially independent of operating temperature

Typical Characteristics

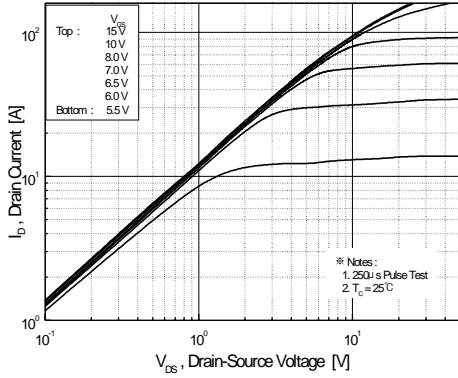


Figure 1. On-Region Characteristics

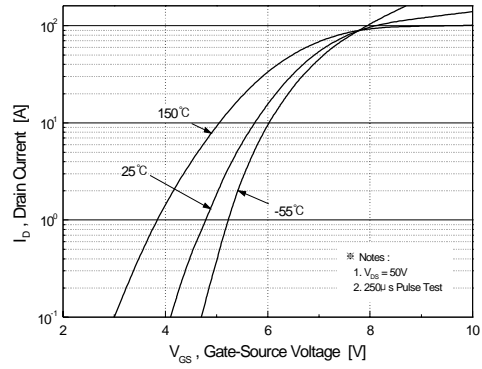


Figure 2. Transfer Characteristics

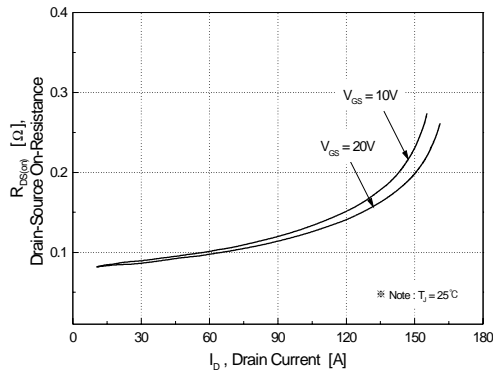


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

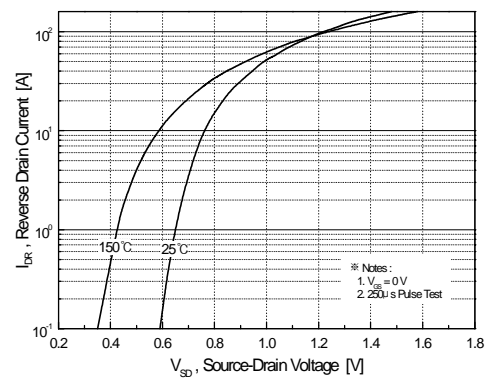


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

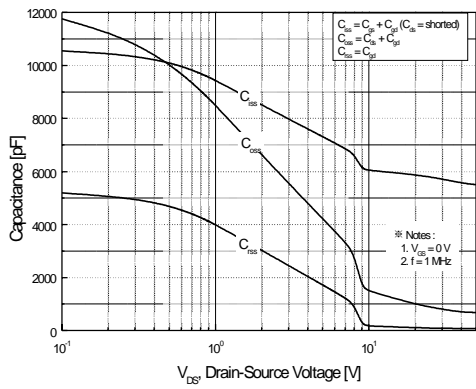


Figure 5. Capacitance Characteristics

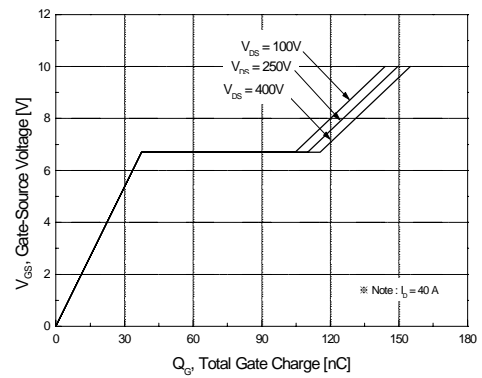


Figure 6. Gate Charge Characteristics

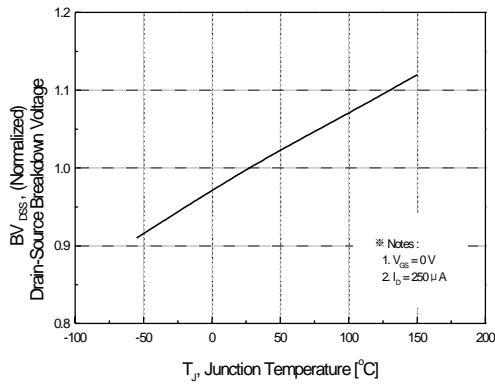


Figure 7. Breakdown Voltage Variation vs Temperature

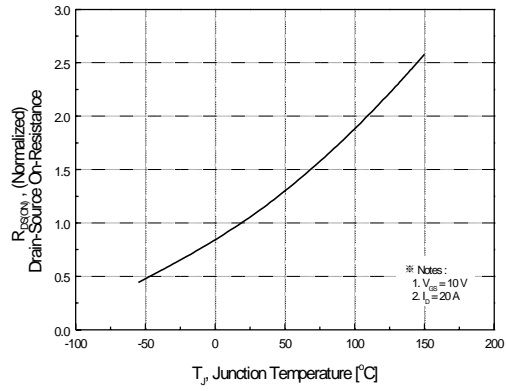


Figure 8. On-Resistance Variation vs Temperature

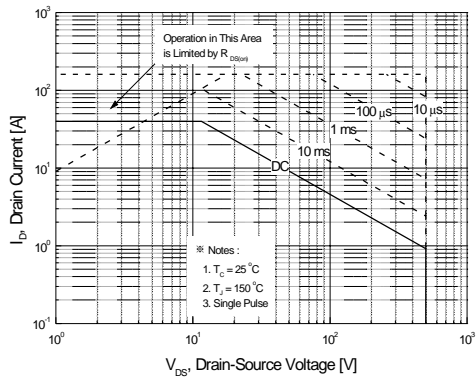


Figure 9. Maximum Safe Operating Area

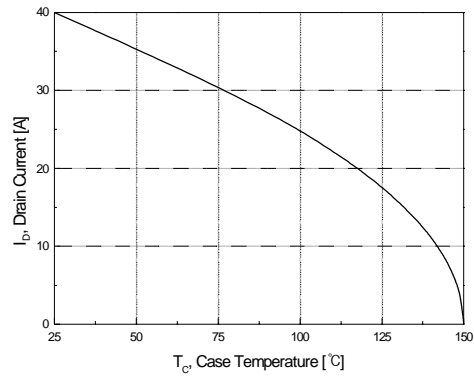


Figure 10. Maximum Drain Current vs Case Temperature

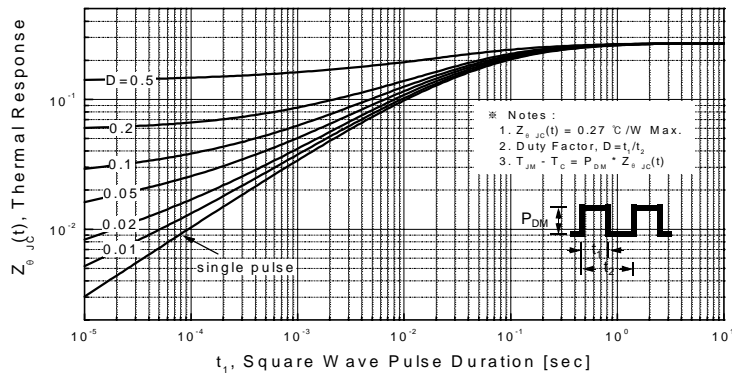


Figure 11. Transient Thermal Response Curve

**Gate Charge Test Circuit & Waveform**



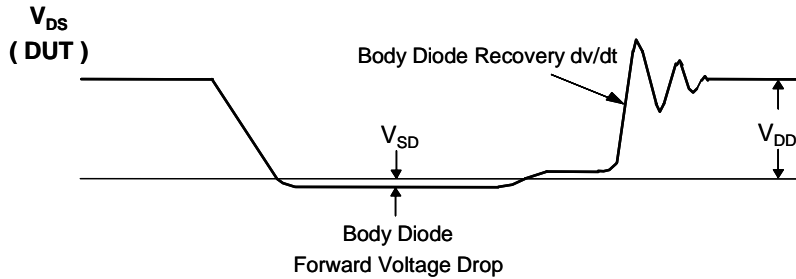
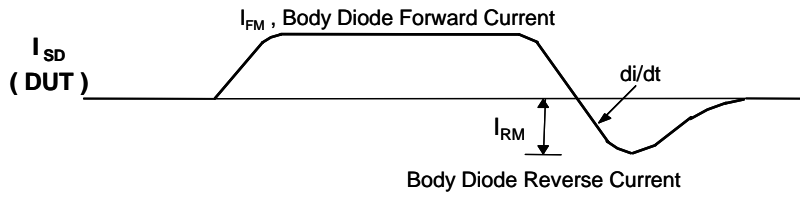
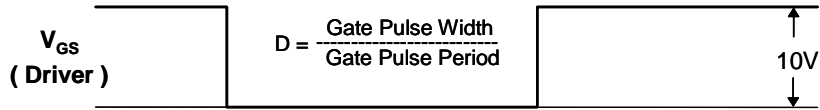
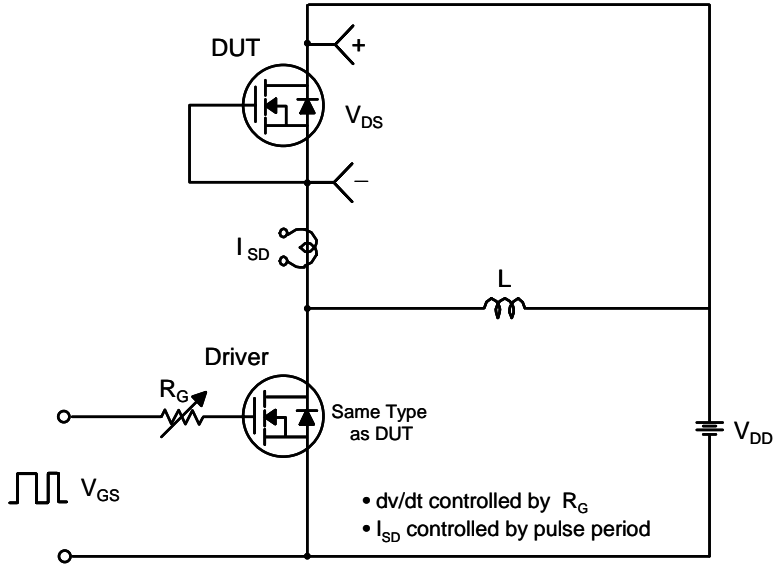
**Resistive Switching Test Circuit & Waveforms**



**Unclamped Inductive Switching Test Circuit & Waveforms**



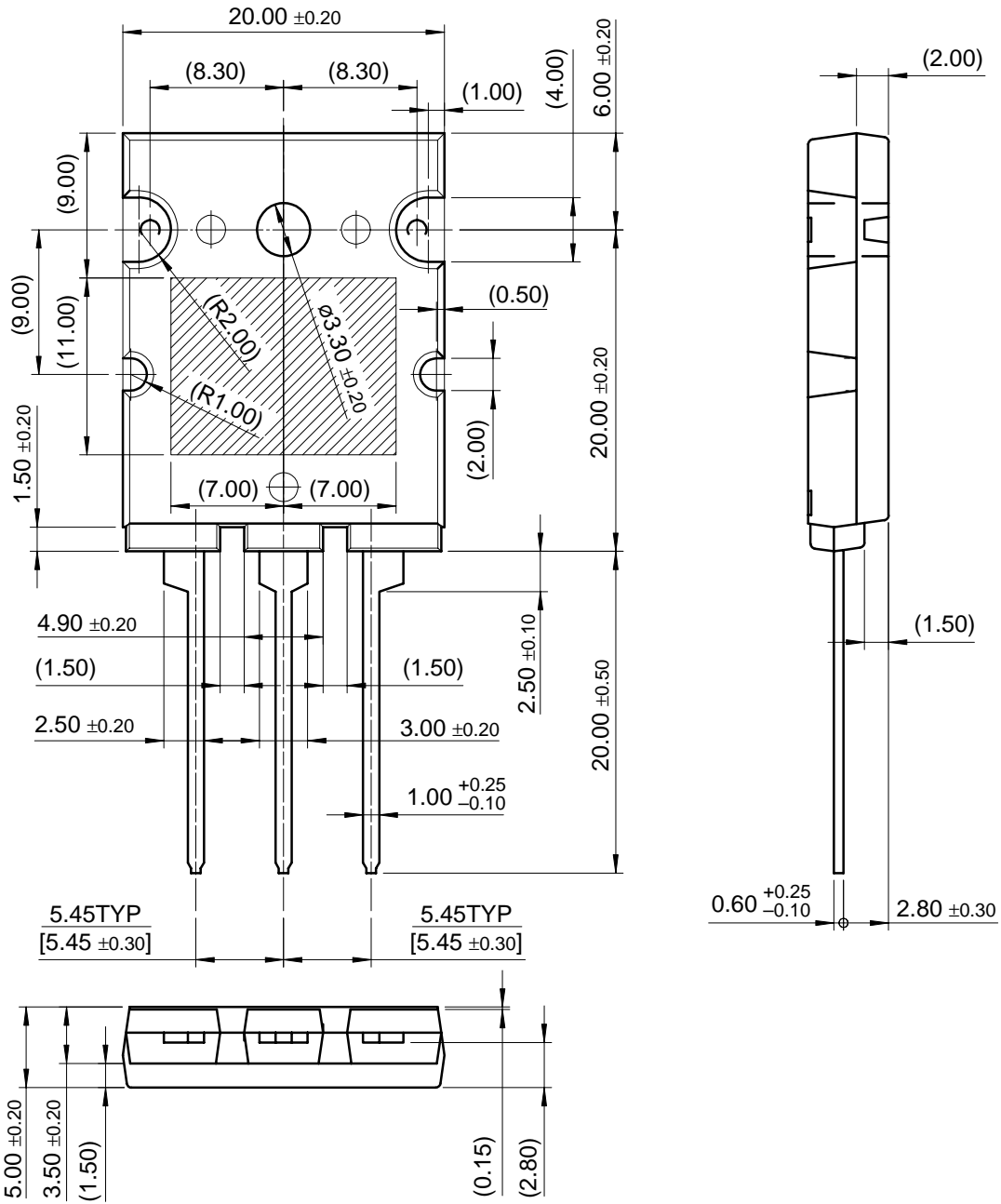
Peak Diode Recovery dv/dt Test Circuit & Waveforms



Package Dimensions

TO-264

FQL40N50F



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